

1.0 INTRODUCTION

High voltage power op amps are often selected to drive capacitive loads, such as **PIEZO TRANSDUCERS, CAPACITORS, ELECTRO-LUMINESCENT DISPLAYS, ELECTROFLUORESCENT LIGHTING, ELECTROSTATIC DEFLECTION**, etc. There are some special considerations when designing circuits to meet your high voltage needs.

We will look in detail at the selection of the power op amp, stability considerations, power dissipation in the op amp and heatsink selection, support components for the circuit, and power supplies and their effect on circuit performance. When we complete these areas of investigation we will look at some alternative power op amp circuits for attaining high voltage control across capacitive loads.

The format of our information will be “definition by example” along with generic formulae for your specific design.

2.0 EXAMPLE DESIGN FOR DRIVING A CAPACITIVE LOAD

GIVEN: +/-Vs= +/-200Vdc

frequency = DC to 10KHz (sinewave)

$V_{IN} = +/-10V$

piezo load with CL = 10.6nF

$V_{OUT} = 360V_{pp}$

Tambient = 25°C, free air convection cooling only

Inverting gain okay

FIND: Power op amp, heatsink and recommended schematic for piezo drive.

SOLUTION: Sections 2.1 thru 2.6 will provide a detailed, logical approach to designing a solution for this capacitive load drive problem.

2.1 POWER OP AMP SELECTION

STEP 1: Define capacitive load. Here we are given CL = 10.6nF

STEP 2: Calculate large signal response (slew rate) using highest frequency and largest voltage swing. The required slew rate to track a sinewave at a given frequency for a given output amplitude is as follows:

$$S.R. = 2 \pi f V_{op} (1 \times 10^{-6})$$

$$\text{Slew Rate [V/}\mu\text{s]} = 2 \times \pi \times \text{frequency} \times V_{OUT \text{ peak}} \times (1 \times 10^{-6})$$

$$S.R. = 2 \pi 10\text{KHz} 180 (1 \times 10^{-6}) = 11.3\text{V}/\mu\text{s}$$

STEP 3: Calculate maximum current requirements. This will occur at highest frequency with capacitive loads.

METHOD 1: Calculate Xc @ highest frequency.

$$X_c = \frac{1}{2 \pi f CL}$$

$$X_c = \frac{1}{2 \pi 10 \text{ KHz } 10.6\text{nF}} = 1.5\text{K}\Omega$$

$$I_{op} = \frac{V_{op}}{X_c} = \frac{180\text{V}}{1.5\text{K}\Omega} = 120\text{mA}$$

METHOD 2: Use highest slew rate and largest voltage swing

$$I_{op} = CL \frac{dV}{dt}$$

$$I_{op} = 10.6\text{nF} \frac{11.3\text{V}}{\mu\text{s}} = 120\text{mA}$$

STEP 4: Do a first pass worst case power dissipation calculation. For details on derivation of this formula see “General Operating Considerations.”

$$P_{DOUT \text{ max}} = \frac{V_s^2}{2 Z_L} \left[\frac{4}{\pi} - \cos \Theta \right]$$

For capacitive load applications this formula reduces to:

$$P_{DOUT \text{ max}} = \frac{4 V_s^2}{2 \pi X_c} = \frac{4 (200)^2}{2 \pi 1.5\text{K}\Omega} = 17\text{W}$$

STEP 5: Summarize what we know and pick power op amp.

+/-Vs = +/-200Vdc

S.R. = 11.3V/μs

I_{op} = 120mA

V_{op} = 180Vp

P_{DOUT MAX} = 17W

In viewing the APEX High Voltage Selector Guide there is only one likely candidate for this design—PA85.

STEP 6: Review the chosen amplifier’s data sheets for details.

Figure 1: Contains relevant excerpts from the PA85 data sheet.

Figure 1A: From the output specifications, a worst case saturation voltage of 10V at 200mA is identified. Therefore we can meet 180Vp out at 120mA without a problem.

Figure 1B: From the power response curve we see 360Vpp at 10KHz is within the power response curve for any value of Cc (PA85 compensation capacitor).

Figure 1C: Since we want 180Vp out for 10Vp in we will be operating at a gain of 18. This is close enough to 20 to choose Cc = 10pF and Rc = 330Ω. This will maximize small signal bandwidth as well as slew rate should a last minute decision require more performance out of the design.

Figure 1D: At Cc = 10pF the slew rate is about 400V/μs, so there is no question about meeting the requirement for an 11.3V/μs slew rate.

Figure 1E: At a closed loop gain of 18, (25 dB), it can be determined that for Cc = 10pF the closed loop bandwidth of this circuit (fcl) is about 2MHz. This first check says not only can a 10KHz sinewave be tracked in the large signal domain, but the PA85 will also have enough bandwidth to have a flat response at 10KHz in the small signal domain.

Figure 1F: From our previous calculation P_{DOUT MAX} = 17W. An Applications Engineer’s rule of thumb for power derating curves works as follows:

For a 25°C ambient temperature you can find a heatsink that will allow you to keep the case temperature at 85°C using free air convection cooling.

Therefore, 17W output power dissipation almost intersects with the $T_c = 85^\circ\text{C}$ line on the power derating curve. This means our first look says we should be able to heatsink the

PA85 for this design.

Now it would seem the work is done and you can proceed to build a breadboard or commit to printed circuit board layout. But first you must proceed to look at other key issues for driving capacitive loads with power op amps such as stability.

FIGURE 1A

OUTPUT

VOLTAGE SWING
 VOLTAGE SWING
 VOLTAGE SWING
 CURRENT, continuous
 SLEW RATE, $A_v = 20$
 SLEW RATE, $A_v = 100$
 CAPACITIVE LOAD, $A_v = +1$
 SETTLING TIME to .1%
 RESISTANCE, no load

$I_o = \pm 200\text{mA}$
 $I_o = \pm 75\text{mA}$
 $I_o = \pm 20\text{mA}$
 $T_c = 85^\circ\text{C}$
 $C_c = 10\text{pf}$
 $C_c = \text{OPEN}$
 Full Temperature Range
 $C_c = 10\text{pf}$, 2V step
 $R_{CL} = 0$

	MIN	TYP	MAX	UNITS
	$\pm V_s - 10$	$\pm V_s - 6.5$		V
	$\pm V_s - 8.5$	$\pm V_s - 6.0$		V
	$\pm V_s - 7.5$	$\pm V_s - 5.5$		V
	± 200			mA
		400		V/ μs
		1000		V/ μs
	470			pf
		1		μs
		50		Ω

FIGURE 1B

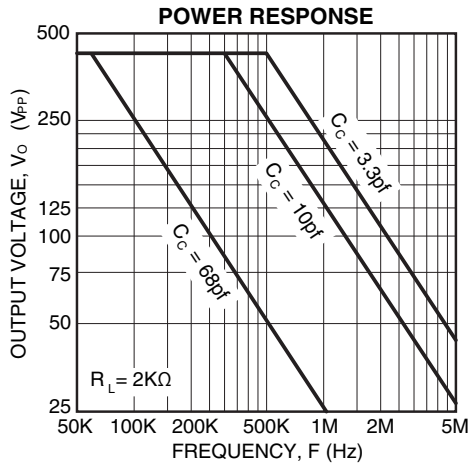


FIGURE 1E

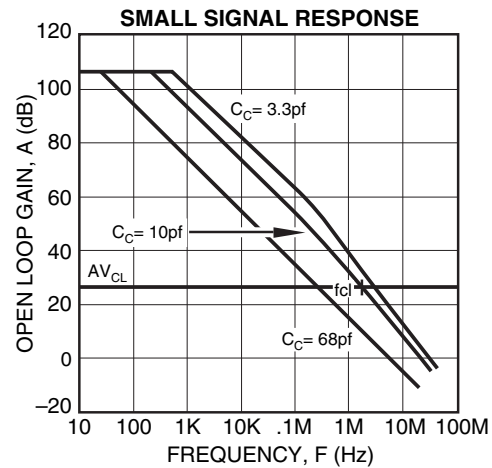
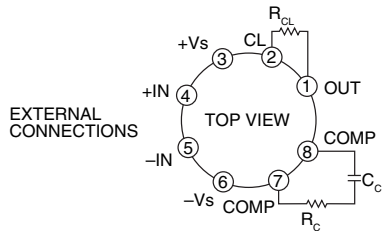


FIGURE 1C



PHASE COMPENSATION

Gain	C_c	R_c
1	68pf	100 Ω
20	10pf	330 Ω
100	3.3pf	0 Ω

C_c RATED FOR FULL SUPPLY VOLTAGE

FIGURE 1D

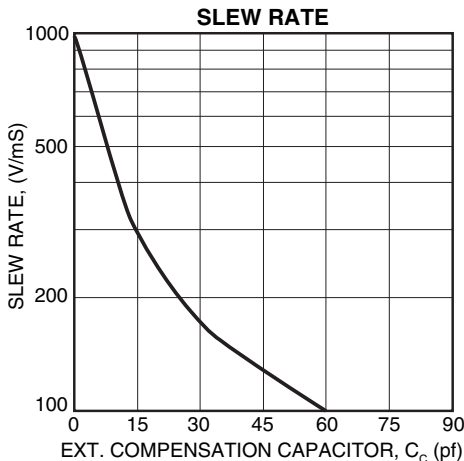


FIGURE 1F

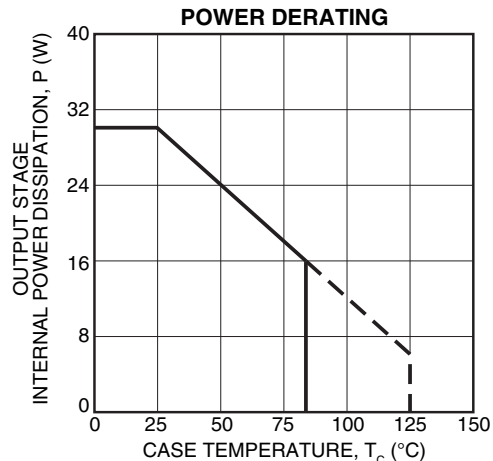


FIGURE 1. PA85 DATA SHEET EXCERPTS

2.2 SMALL SIGNAL STABILITY

Figure 2 is a complete schematic of our PA85 drive circuit. The gain of -18 will give us 360Vpp out for 20Vpp in. We will now look at the details for selecting stability components Rn, Cn, and CF.

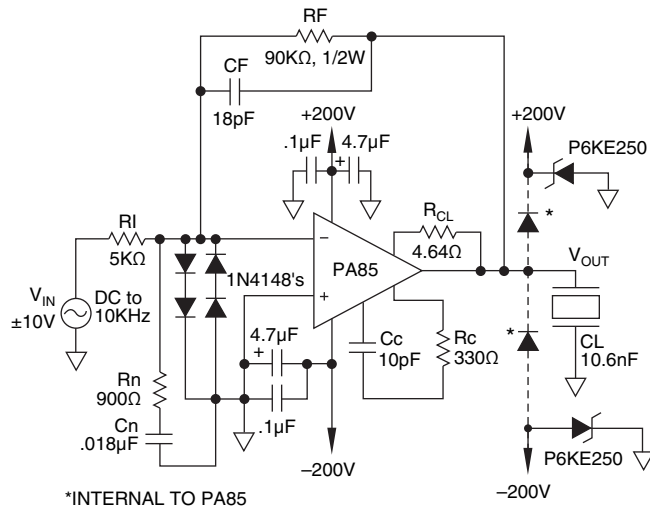


FIGURE 2. PA85 PIEZO TRANSDUCER DRIVE

2.2.1 MODIFIED AOL FOR CAPACITIVE LOADS

Figure 3 illustrates how the amplifier's Aol curve gets modified by Ro, the amplifier's unloaded output impedance, and CL, the capacitive load. Output impedance, Ro, of the amplifier, is flat within the bandwidth of the amplifier and predominantly resistive. Refer to Apex Application Note 19 for a detailed discussion of this issue.

Figure 4 lists high voltage Apex amplifiers and boosters most commonly used to drive capacitive loads and their corresponding output impedance.

OP AMP OR BOOSTER	OUTPUT IMPEDANCE
PA41	150 ohms
PA81J	1.4K-1.8K ohms
PA82J	1.4K-1.8K ohms
PA83	1.4K-1.8Kohms
PA84	1.4K-1.8K ohms
PA85	50 ohms
PA88	100 ohms
PA89	100 ohms
PB50	35 ohms
PB58	35 ohms

FIGURE 4. OUTPUT IMPEDANCE HIGH VOLTAGE OP AMPS AND BOOSTERS

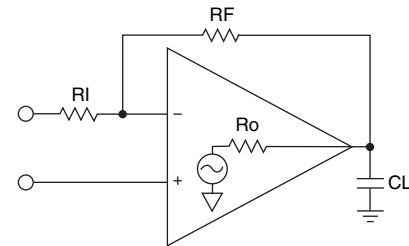
2.2.2 STABILITY PLOTS

Figure 5 illustrates the magnitude plot for stability needed to analyze and check for good stability on our PA85 drive circuit. The low frequency pole for the Aol curve can be determined from the "Small Signal Response" curve, and the high frequency pole can be extrapolated from the "Phase Response" curve in the APEX data sheet for the PA85.

STEP 1: Modify Aol due to capacitive load and amplifier's output impedance:

$$fp2 = \frac{1}{2\pi(Ro + R_{CL})CL} = \frac{1}{2\pi(50\Omega + 4.64\Omega)10.6nF} = 275\text{ KHz}$$

fp4 = 10MHz pole from amplifier's original Aol plot (fp3)



UNITY GAIN STABLE AMPLIFIER
UNSTABLE 40 dB/DECADE WITH CL

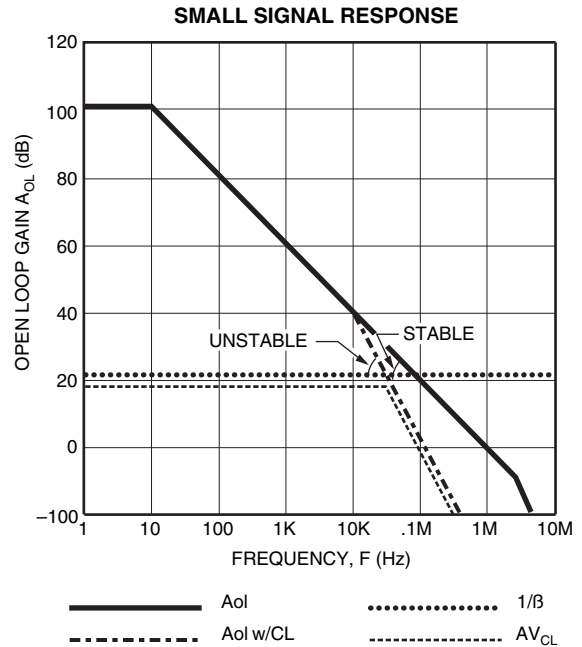


FIGURE 3. CAPACITIVE LOADING

STEP 2: Check 1/B for resistive feedback alone:

1/B [1/(beta)] is the small signal AC gain at which the op amp runs. Refer to Apex Application Note 19 for details. First order stability criteria for magnitude plots states that the Rate-of-Closure (difference between the slopes of Modified Aol and the 1/B plot) be 20dB per decade at fcl. Refer to Apex Application Note 19 for details on Rate-of-Closure. With AC small signal

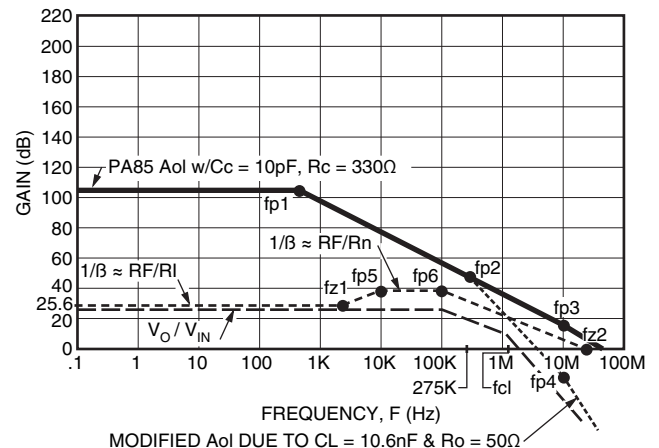


FIGURE 5. MAGNITUDE PLOT FOR STABILITY
(PA85 PIEZO TRANSDUCER DRIVE)

gain set only by RF and RI the 1/β plot will be a flat line at 25.6dB. At the intersection of modified Aol and 25.6dB the Rate-of-Closure will be 40 dB per decade indicating marginal stability and potentially destructive oscillations.

STEP 3: Add Noise Gain Compensation as a first step towards good stability:

Rn and Cn will form a noise gain compensation network which will raise the gain of the 1/β plot without directly affecting the V_{OUT}/V_{IN} relationship. Refer to Apex Application Note 19 for details.

Noise Gain equations:

High frequency gain = $RF/Rn = 90K\Omega/900\Omega = 100 \implies 40dB$

$$fp5 = \frac{1}{2\pi Rn Cn} = \frac{1}{2\pi 900\Omega \cdot 0.018\mu F} = 9.8 \text{ KHz}$$

fz1 \implies Can be obtained graphically using +20dB per decade slope starting at the intersection of fp5 and the high frequency gain of the noise gain compensation and proceeding towards the DC gain.

Even though we have raised the higher frequency portion of the 1/β curve to 40dB, it will still intersect the modified Aol at 40dB per decade Rate-of-Closure.

STEP 4: Add feedback zero (1/β pole) to 1/β plot to gain best AC small signal stability (Refer to Apex Application Note 19 for details):

$$fp6 = \frac{1}{2\pi RF CF} = \frac{1}{2\pi 90k 18pF} = 98 \text{ KHz}$$

Now at fcl, you have the desired 20dB per decade Rate-of-Closure and good stability according to our first order criteria for magnitude plots. You will now need to plot the open loop phase plot for a complete stability check.

STEP 5: Review of rules for open loop phase plots:

- 1) Poles in the 1/β plot become zeros in the open loop stability check.
- 2) Zeros in the 1/β plot become poles in the open loop stability check.
- 3) Poles and zeros in the Aol curve or modified Aol curve of the op amp remain respectively poles and zeros in the open loop stability check since the op amp Aol curve is an open loop curve already.
- 4) Phase for zeros is represented by a +45 degree phase shift at the frequency of the zero with +45 degree per decade slope, extending this line with 0 degree and +90 degree horizontal lines.
- 5) Phase for poles is represented by a -45 degree phase shift at the frequency of the pole with a -45 degree per decade slope, extending this line with 0 degree and -90 degree horizontal lines. Refer to Apex Application Note 19 for further details.

STEP 6: Plot open loop phase using information from magnitude plot: Figure 6 is the open loop phase plot for our PA85 drive circuit.

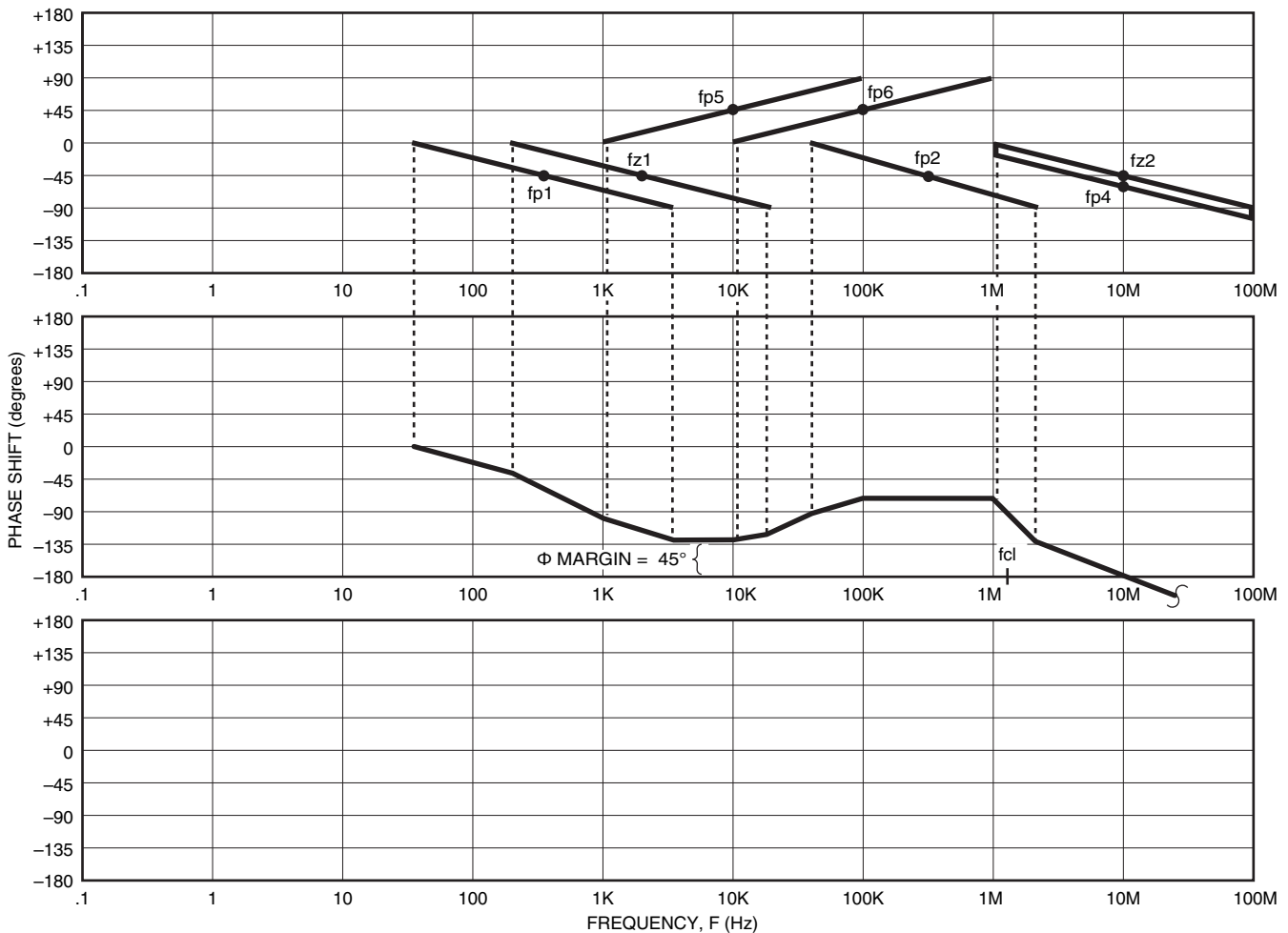


FIGURE 6. OPEN LOOP PHASE CHECK FOR STABILITY (PA85 PIEZO TRANSDUCER DRIVE)

Notice in Figure 5 that the 1/β plot continues beyond f_{cl} all the way until it intersects at 0dB forming f_{z2} in the 1/β plot. An amplifier will not run in an AC small signal gain of less than 0dB. You must account for an additional high frequency pole in the open loop phase check. This pole is easily read graphically from Figure 5 rather than calculating it from lengthy derivations.

A review of Figure 6 shows graphical addition of the contributions from all poles and zeros to yield a net open loop phase plot. The phase margin from DC to f_{cl} is never less than 45 degrees which implies good stability for this circuit.

2.2.2.1 RULES OF THUMB FOR STABILITY PLOTS

Now that we know we have good stability, let's return to the magnitude plot in Figure 5 for a few handy rules of thumb:

- 1) Think of open loop phase when play with the 1/β plot: Notice that fp1 (pole in open loop) is spaced about a decade away from fz1 (pole in open loop). If you don't add fp5 (zero in open loop) within a decade of fz1, (pole in open loop) the open loop phase margin will dip to less than 45 degrees.
- 2) As you run out of loop gain (difference between Aol curve and 1/β plot), keep poles and zeros one-half to one decade away from zero loop gain. Notice that fp6 is about one-half decade away from the modified Aol curve near fp2. This allows "Real World" Aol curves and component tolerances to stack against you without creating stability nightmares.
- 3) Always design your circuits, using these stability techniques, for 45 degrees of phase margin in the open loop phase check for stability. This is because the first order linear approximations for phase have a six degree error. As well, there is no guarantee you will consistently receive op amps with the typical Aol graph.

In a typical design procedure, you will plot magnitude plots for stability first, do an open loop phase plot, and then return to calculate final component values to create the desired magnitude plot that yields 45 degrees open loop phase margin for stability.

Refer to Apex Application Note 19 for handy tips and short cuts for plotting magnitude and phase plots.

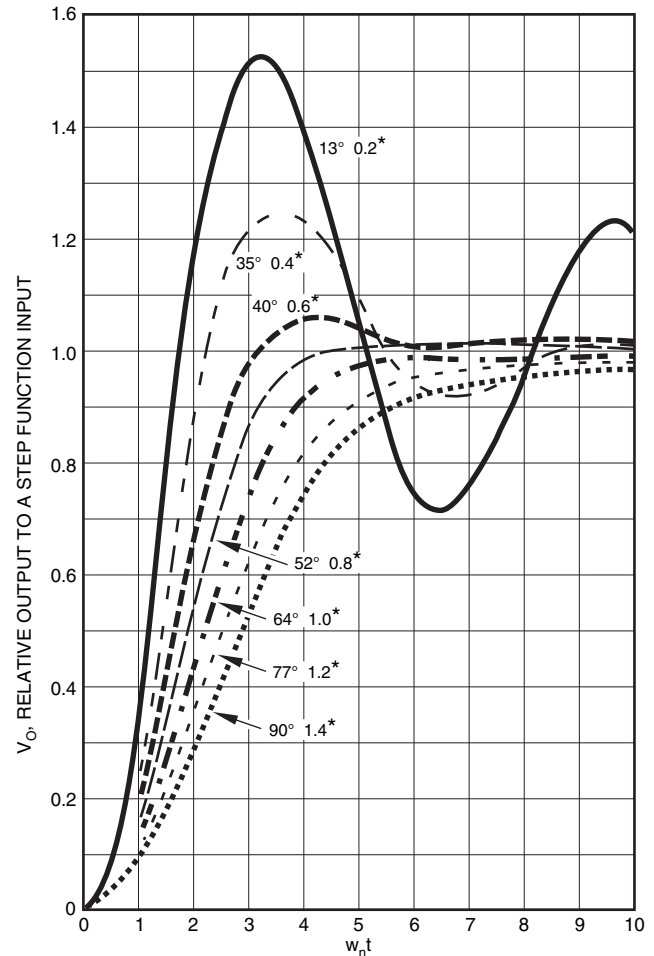
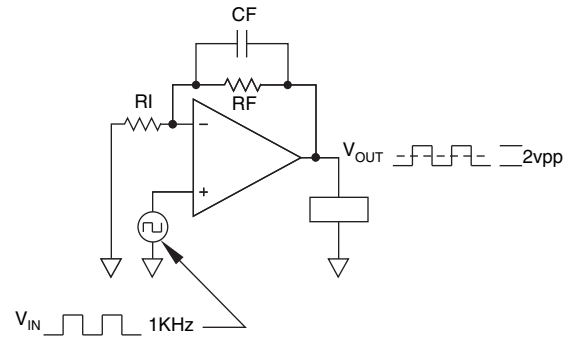
2.2.2.3 "REAL WORLD" STABILITY TEST

Once a circuit is built, there is a relatively easy test you can run to verify if the predicted open loop phase margin made it from design to the "real world".

Figure 7 details the Square Wave Test for measuring open loop phase margin by closed loop testing. The output amplitude of the square wave is adjusted to be 2V_{pp} at a frequency of 1 KHz. The key elements of this test are to use low amplitude (AC small signal) and a frequency that will allow ease of reading when triggered on an oscilloscope. Amplitude adjustment on the oscilloscope wants to accentuate the top of the square wave to measure easily the overshoot and ringing. The results of the test can then be compared to the graph in Figure 7 to yield a reading for open loop phase margin.

A complete use of this test is to run the output symmetrical about zero with +/-1V peak and then re-run the test with various DC offsets on the output above and below zero. This will check stability at several operating points to ensure no anomalies show up in field use.

Refer to Apex Application Note 19 for more involved closed loop tests for measuring open loop phase margin and checking "real world" stability.



* OPEN LOOP PHASE MARGIN AND DAMPING FACTOR

FIGURE 7. SQUARE WAVE TEST

2.3 CLOSED LOOP RESPONSE

From Figure 5 the V_{OUT}/V_{IN} relationship for our PA85 circuit is seen as flat from DC to 100 KHz, where it begins to roll at 20dB per decade. It continues until we reach 1.33 MHz where it rolls off at 40dB per decade until reaching 10MHz, where our slope changes to 60dB per decade.

The V_{OUT}/V_{IN} phase shift for any given frequency is given by the following:

$$\text{Phase Shift} = -\tan^{-1} \frac{f}{fp6} - \tan^{-1} \frac{f}{fcl} - \tan^{-1} \frac{f}{fp4}$$

where f = frequency of interest for phase shift

For our upper frequency of interest of 10 KHz let's see what the V_{OUT}/V_{IN} phase shift is:

$$\text{Phase Shift} = -\tan^{-1} \frac{10 \text{ KHz}}{100 \text{ KHz}} - \tan^{-1} \frac{10 \text{ KHz}}{1.33 \text{ MHz}}$$

$$-\tan^{-1} \frac{10 \text{ KHz}}{10 \text{ MHz}} = -6.2 \text{ degrees}$$

The formula above can be expanded to include any number of poles. If the V_{OUT}/V_{IN} relationship has zeros simply add the following for each zero:

$$+\tan^{-1} \frac{f}{f_z}; \text{ where } f_z \text{ is the frequency of the zero}$$

2.4 POWER DISSIPATION AND HEATSINKING

Power dissipation inside the amplifier consists of two components, P_{DQ} , quiescent power dissipation, and P_{DOUT} , output stage power dissipation. Simply compute $P_{DQ} = I_Q[+V_S - (-V_S)]$ and add the worst case power dissipation for the output stage to this to form P_{DINT} , total internal power dissipation. Figure 8 shows the Thermo-Electric Model that is applicable for this situation.

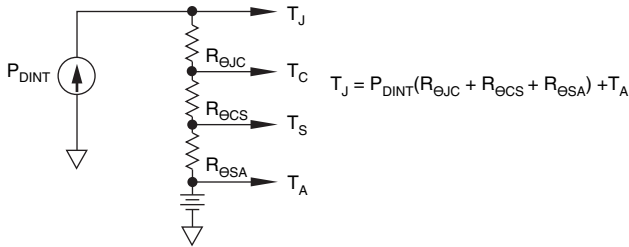


FIGURE 8. THERMO-ELECTRIC MODEL

In our PA85 design case we have AC power dissipation in the output stage. From Section 2.1, Step 4, that power dissipation is:

$$P_{DOUT \text{ max}} = \frac{4 V_S^2}{2 \pi X_C} = \frac{4 (200)^2}{2 \pi 1.5 \text{ K}\Omega} = 17 \text{ W}$$

Quiescent power is:

$$P_{DQ} = I_Q [+V_S - (-V_S)] = 25 \text{ mA} [+200 - (-200)] = 10 \text{ W}$$

There are two thermal requirements we must meet in this application. First, the case temperature must be kept below 85°C. Second, the junction temperature must be kept below 150°C. We know the application is dissipating a total of 27W, but the data sheet contains three different thermal resistance ratings which vary substantially. The first is an AC rating where the two output transistors share the heat load at a frequency of 60Hz or greater. When the power is dissipated in mainly one output transistor, use the DC thermal resistance. The last rating is applied only if no heatsink is used.

This is a rare practice with power op amps. Let us briefly pursue the possibility we might be able to not heatsink the amplifier in this application. Figure 9 models this case. TO-3 packages are rated at 30°C/W. When the case of the amplifier

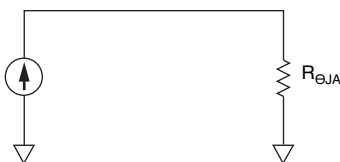


FIGURE 9. THERMO-ELECTRIC MODEL (NO HEATSINK)

must be kept below 85°C, this imposes a maximum power dissipation of 2W even with an ideal ambient temperature of 25°C. At 27W our PA85 would burn up very quickly without a heatsink.

The PA85 data sheet tells us the AC thermal resistance is 2.5°C/W. We will allow 0.2°C/W for $R_{\theta_{CS}}$ and use the following to determine a maximum heatsink rating.

$$R_{\theta_{SA}} \frac{T_J - T_A}{PD_{INT(\text{max})}} - R_{\theta_{JC}} - R_{\theta_{CS}}$$

$$\frac{(150 - 25)^\circ\text{C}}{27 \text{ W}} - 2.5^\circ\text{C/W} - 0.2^\circ\text{C/W}$$

$$R_{\theta_{SA}} \quad 1.9^\circ\text{C/W}$$

Select APEX HS03; $R_{\theta_{SA}} = 1.7^\circ\text{C/W}$ with forced air flow at 100 ft/min.

As a last check, multiply the total power times the sum of the thermal resistance of the heatsink and the mounting interface and add to ambient temperature to verify the case temperature does not exceed 85°C.

$$27 \text{ W} \cdot (1.7^\circ\text{C/W} + 0.2^\circ\text{C/W}) + 25^\circ\text{C} = 76.3^\circ\text{C}$$

Refer to "Package and Accessories Information" section of APEX Amplifier Handbook. See APEX catalog "GENERAL OPERATING CONSIDERATIONS" for details on heatsinking and mounting the amplifier.

2.5 HIGH VOLTAGE AMPLIFIER SUPPORT COMPONENTS

High voltage op amps require some special considerations when selecting support components for completion of your circuit design. The following list covers these critical areas of concern:

1) ESD Handling Precautions:

All APEX high voltage amplifiers are rated Class 1 for ESD sensitivity, as defined in MIL-H-38534. This requires that proper ESD handling precautions be observed from receiving through manufacturing until the device is installed in a properly designed circuit. Areas which will require strict ESD control include, but are not limited to, personnel, tabletops, stocking containers, floors, soldering irons, and test equipment.

2) Input Protection (Refer to Figure 10):

Most high voltage amplifiers have a differential input voltage rating of +/-25V. It is easier on high voltage amplifiers to cause differential input overvoltages than on lower voltage op amps. These overvoltages on the input can occur during power cycling or can be transients fed back through CF from the output to the input.

The input diodes, D_p , clamp the maximum input differential voltage to +/-1.4V while allowing sufficient differential voltage for overdrive when demanding maximum slew rate from the amplifier. The diodes shown are low capacitance fast signal diodes. If lower leakage and lower capacitance diodes are desired, J-FETs may be connected as diodes as shown.

3) Output Diodes (Refer to Figure 10):

MOSFET high voltage amplifiers have internal, intrinsic diodes that are connected from the output to each supply rail. High voltage Bipolar amplifiers do not have these diodes and must be added externally as shown. The MOSFET amplifiers' internal diodes are sufficient for an occasional transient that may be created in a piezo drive situation where the piezo element is stressed mechanically, thereby creating an electrical voltage. For applications where there is poten-

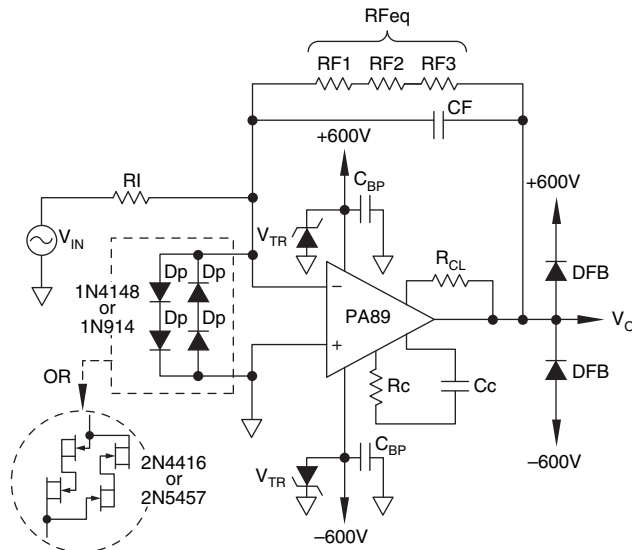


FIGURE 10. HIGH VOLTAGE SUPPORT COMPONENTS

tial for sustained high energy flyback, in ATE applications, where everything that is not supposed to happen usually can and does, or in applications where Kilovolt flashovers can occur and be impressed onto the amplifier's output, it is recommended to use fast (500nS or less depending upon the anticipated flyback energy frequency) reverse recovery diodes, DFB, external to the amplifier. Remember to size the diodes for a Peak Reverse Voltage rating of at least the rail to rail supplies the amplifier is operating at (for $V_s = \pm 200V \implies 400V$ Peak Reverse Voltage rated diode).

4) Transient Voltage Suppressors (See Figure 10):

Transient Voltage Suppressors, V_{TR} , can be added to the supply lines to provide protection from undesired transients on the power supply line. The first is power supply overvoltage on power cycling. Secondly, when energy is dumped into the supplies from DFB, if the power supply terminals at the amplifier do not look like a low impedance for the frequency of that energy, the amplifier could become overvoltage. Transient suppressors, such as TRANSZORBs, manufactured by General Semiconductor Industries, Inc, will provide a low impedance path for this energy. If you use unipolar transient suppressors, they will prevent polarity reversal across the amplifier since they will become a forward biased diode if supplies are reversed.

Selection of the transient suppressors may require a series string of devices to reach the desired reverse stand-off voltage rating for higher voltage op amps. Choose the transient suppressor for a reverse stand-off voltage slightly greater than the maximum DC or continuous peak operating voltage level. This selected device will then have an actual breakdown voltage that is typically 1.1 to 1.36 times higher. For example, a P6KE250 has a reverse stand-off voltage of 202V with a breakdown voltage of 225V to 275V. Herein lies the trade-offs of transient suppressors. They are excellent devices with a sharp breakdown curve and can dissipate large amounts of power for short periods of time. The problem is the exact breakdown voltage is not a tightly controlled parameter for any given model.

A typical design dilemma is the case where an engineer desires to use a part at its full power supply rating and still provide transient voltage protection on the supply lines. Now you ask, how high is APEX's Absolute Maximum Rating for Supply Voltage, REALLY? Well, the guaranteed Absolute Maximum Rating for Supply Voltage is exactly what our

vendors guarantee to us. Lawyers aside, it is known in the electronics industry that a 400V transistor may actually breakdown at 500V from a given lot. In a nutshell, you are in no-man's land above the Absolute Maximum Rating; however, it is much better to limit the transient voltages to as low as possible than to not limit at all!

5) Power Supply Bypassing (See Figure 10):

The rule of thumb is .1 μ F ceramics directly at the op amp with 10 μ F/Ampere of peak output current in parallel within 2 inches or so of each amplifier. Many of the high voltage amplifiers are less than 200mA and the .1 μ F ceramic is all that will be needed. In cases of PA89, +/600V supplies, .01 μ F seems to be more readily available and this is adequate for high frequency bypassing on the power supply line. Watch the voltage ratings for these capacitors!

6) Compensation Capacitor and Resistor (See Figure 10):

C_c must be rated for the rail-to-rail supply voltage at which the amplifier is operating. In this case a 1200V rating. It is recommended that the compensation capacitor be a temperature stable capacitor for reliable performance over temperature. Mepco / Centralab, Inc, series D and S type capacitors are available in 50Vdc through 6KVdc ratings in various temperature characteristics.

R_c will normally see little or no voltage since most of the voltage stresses will be across C_c . R_c then can be a standard 1/8W metal film resistor.

7) Feedback and Input Components (See Figure 10):

R_I will generally have little voltage stress or power dissipation since most input signals are less than 10 volts peak. Standard metal film resistors will work fine.

C_F can have up to one supply impressed across it. In this case it would need to be a 600Vdc minimum rated capacitor.

$RF1$, $RF2$, and $RF3$ will need some special considerations. Power dissipation will become of prime importance since up to one of the supply rails can be impressed across these resistors at a given time. This could yield power dissipations of: $P_D = V_s^2 / R_{FEq}$. The second consideration is voltage coefficient of resistance. This is a parameter that defines how a resistor changes its resistance with applied voltage. At low voltages this characteristic is not a dominant factor. At higher voltages it can become a more significant factor causing reductions in gain for a given resistor ratio or increased distortion. Dale RNX, ROX, FHV, MVW, and HVX series resistors are well characterized for high voltage use. The power dissipation factors and voltage coefficient of resistance may require several resistors to be used in series in the feedback path of the op amp.

8) Current Limit Resistor (See Figure 10):

Remember that all the load current flows through the current limit resistor, R_{CL} , and therefore size it according to the value of current limit, I_{lim} , by $P_D = (I_{lim}^2)(R_{CL})$. Maximum voltage stress across R_{CL} will be about +/- .7V for most amplifiers. Check the "Current Limit" section of the applicable data sheet for exceptions to this.

9) PWB Layout:

Higher voltages will require wider spacings between traces on a printed circuit board layout as well as spacings between ground planes and other conductive layers. Mil-Std-275 provides some guidelines in these areas.

10) Probing, Plugging and Powering:

Be extremely careful when probing a high voltage amplifier with the power on. An inadvertent slip of a probe can destroy a high voltage amplifier. There are often compensation pins adjacent to power supply pins. Those compensation pins are often connected to the gates of MOSFETs which do not

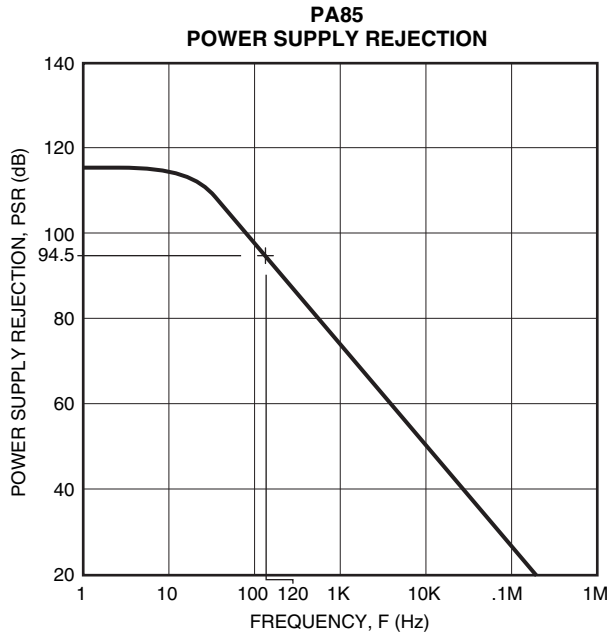


FIGURE 11. PA85 PSR

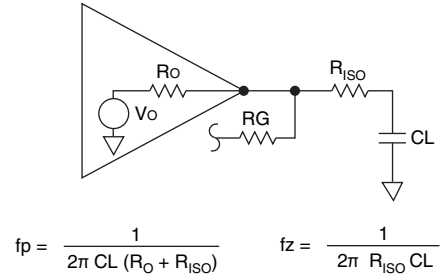


FIGURE 12A: R_{iso} & CL

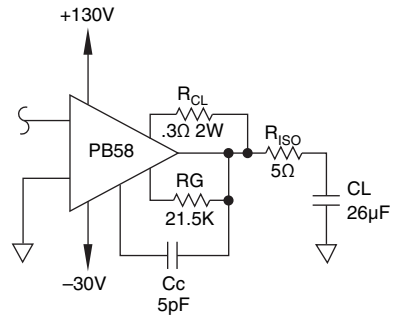


FIGURE 12B: PB58 w/ R_{iso} & CL

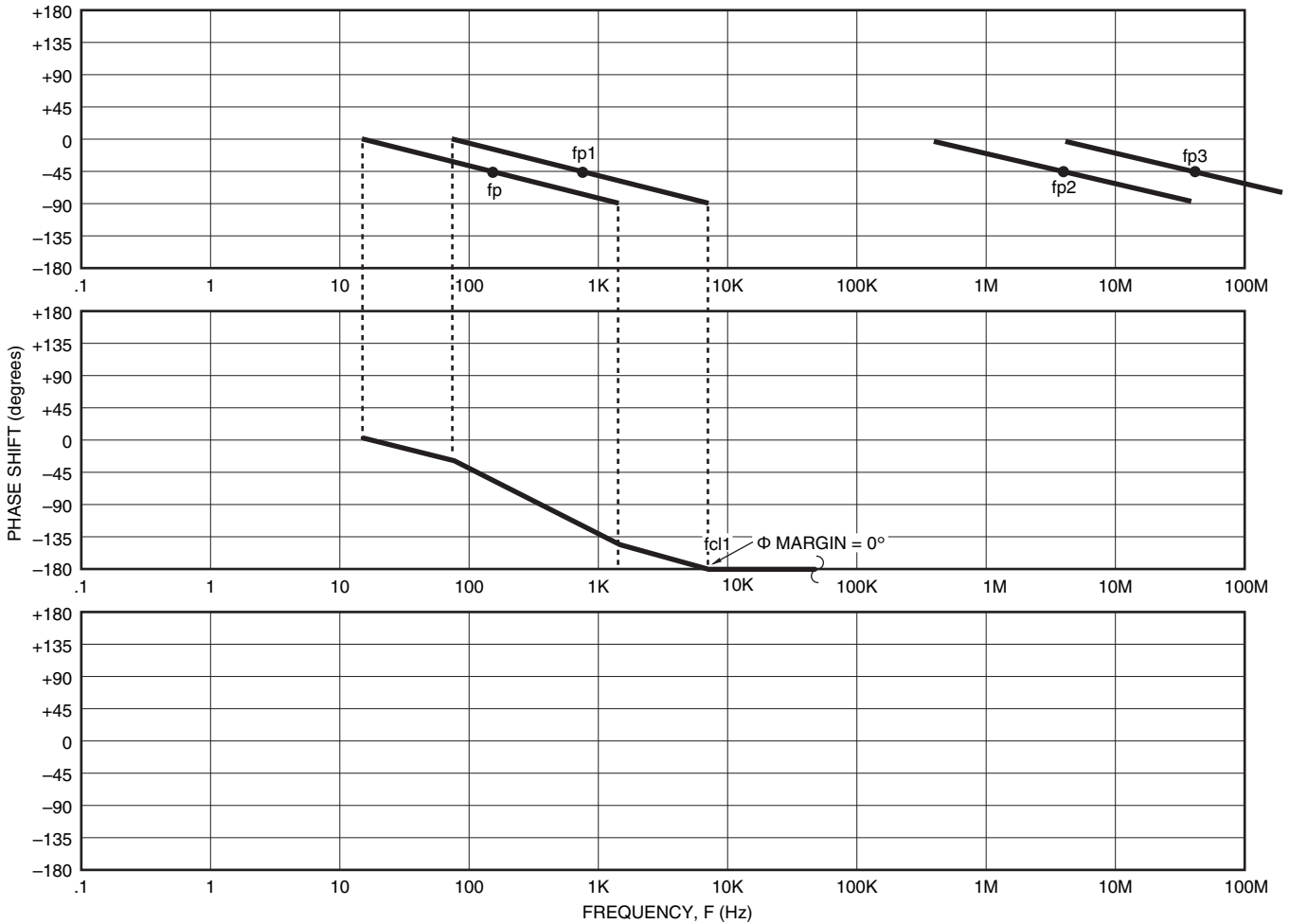


FIGURE 14. OPEN LOOP PHASE PLOT FOR STABILITY CURVE ① (w/o R_{iso})

take kindly to the full power supply being impressed upon them.

Do not plug or unplug an amplifier into a live, powered socket. The transients generated can destroy the high voltage amplifier.

Do not use fuses in the power supply lines of high voltage amplifiers or ever power them with one supply disconnected and no path to ground for that disconnected power supply. This can lead to a sneak path for permanent destruction on several of the high voltage amplifiers.

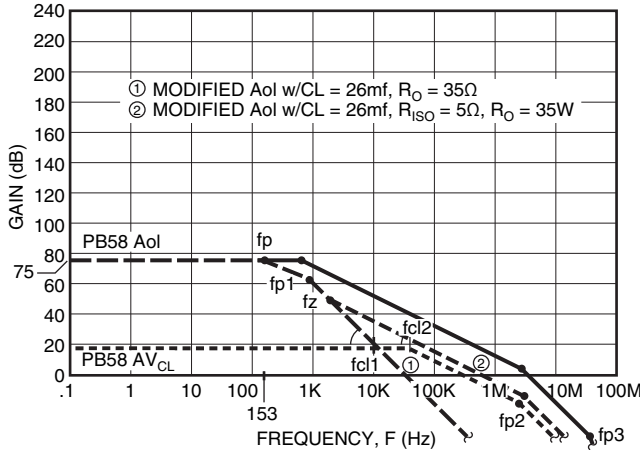


FIGURE 13. R_{ISO} & CAPACITIVE LOAD EFFECTS

2.6 POWER SUPPLIES

2.6.1 POWER SUPPLY REJECTION

Often times high voltage amplifiers require the use of either a switching power supply or a simple AC full-wave bridge rectified supply (make real sure you use transient suppressors if you use this type of supply). The question then is asked what will be the effect on the output of the amplifier due to the ripple of the power supply?

Figure 11 (previous page) is the Power Supply Rejection curve for the PA85. We will use this and our familiar circuit of Figure 2 to understand power supply ripple effect on amplifier output. Figure 11 is a referred-to-input specification. Let's assume there is a 1Vpp, 120Hz ripple on the power supply line. From Figure 11 this implies PSR of 94.5dB. Since this is a rejection curve, the gain is actually -94.5dB which is a gain of .000018836. This gain times 1Vpp on the power supply line means you will see .018836mVpp appear as an input offset voltage in the circuit. At a gain of 19 this means our output will see .358mVpp ripple at 120Hz due to power supply fluctuations.

2.6.2 HIGH VOLTAGE POWER SUPPLIES

See the last few pages of the ACCESSORIES INFORMATION data sheet for a list of manufacturers of high voltage supplies. As a group, these vendors offer AC and DC inputs, standard and custom units in linear and switching topologies. No matter what supply you use, check it for possible overshoot

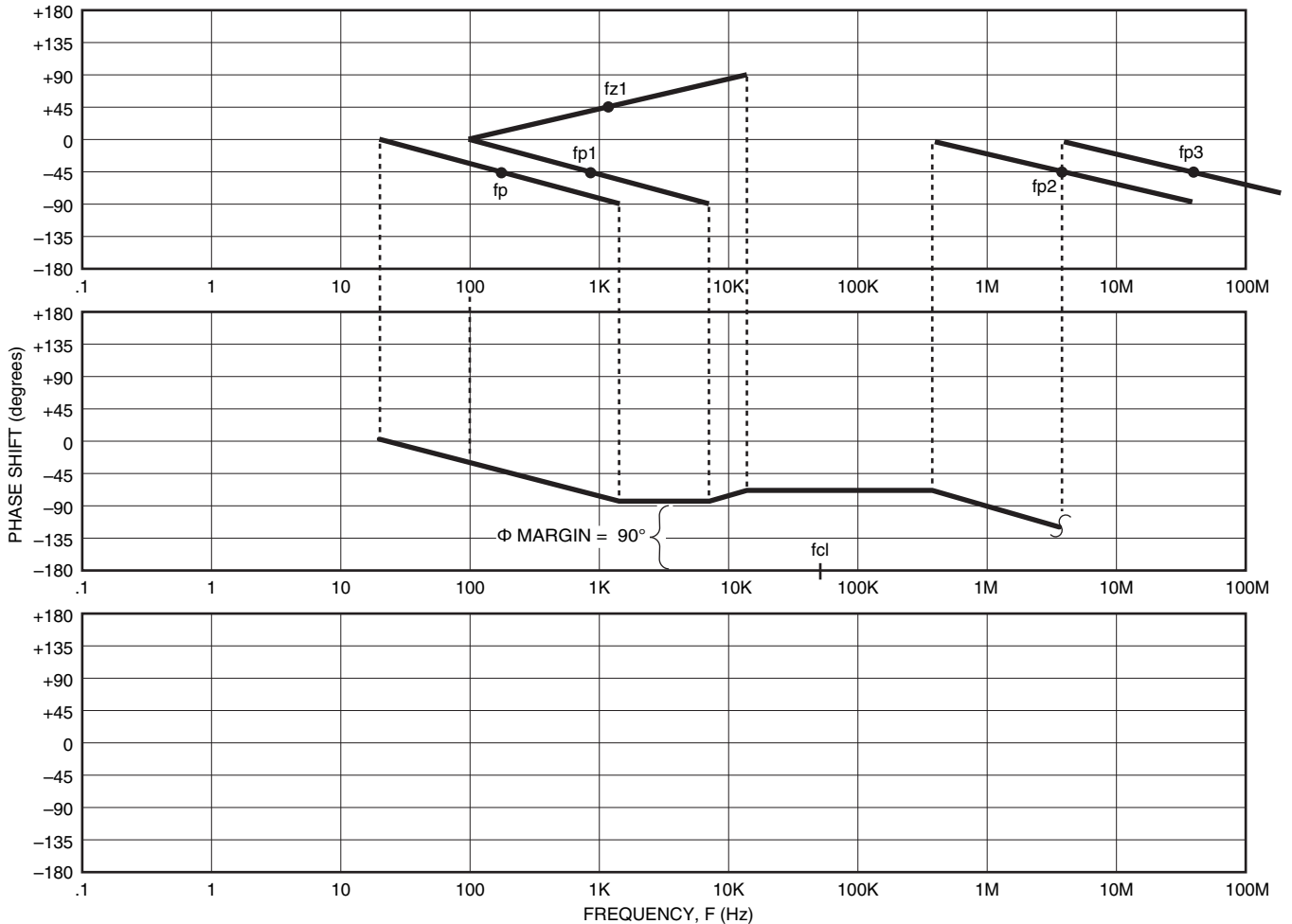


FIGURE 15. OPEN LOOP PHASE PLOT FOR STABILITY CURVE ② (w/ R_{ISO})

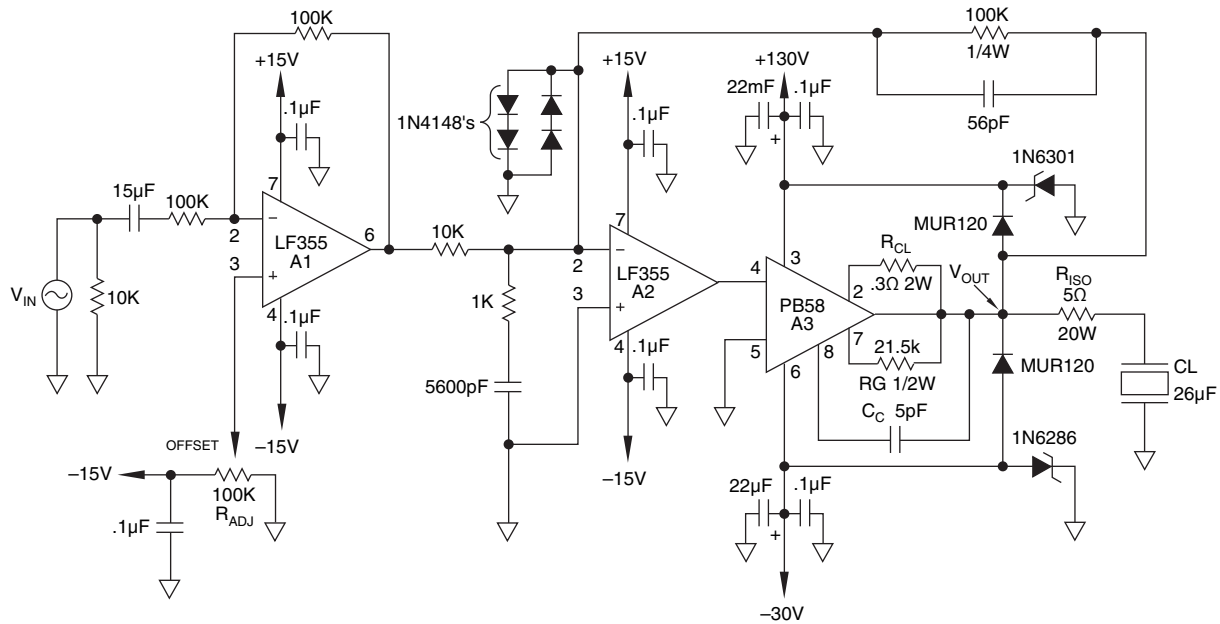


FIGURE 16. PB58 PIEZO DRIVE w/R_{ISO}

at power up, power down and even power cycling. Beware that many high voltage supplies feature foldback or foldover current limiting. In these circuits, current limit is reduced at low voltages compared to full output voltage. Current sources in Apex high voltage amplifiers draw their rated quiescent current at somewhere around half their minimum supply voltage rating. For example, the PA85 is likely to draw over 20mA as soon as the supplies reach +/-7 to 10V. If a foldback feature does not allow this operating point, the system will latch up.

3.0 HIGH VOLTAGE AMPLIFIER VARIATIONS

3.1 RESISTOR ISOLATION FOR CAPACITIVE LOADS

In Section 2.2.2 one method for stabilizing capacitive loads was discussed. There is another common way to isolate capacitive loads and thereby acquire good stability.

Figure 12A (back 2 pages) illustrates a technique for isolating the capacitive load through the use of R_{ISO}. This isolates the point of feedback, where RG is connected, from the capacitive load. The addition of R_{ISO} adds a zero in the modified Aol plot to counteract the pole formed by Ro and CL. Figure 12A also contains the equations for the modified Aol curve defining fp and fz.

Figure 12B (back 2 pages) will be part of a real world design for a PIEZO DRIVE CIRCUIT. Here a PB58 will be required

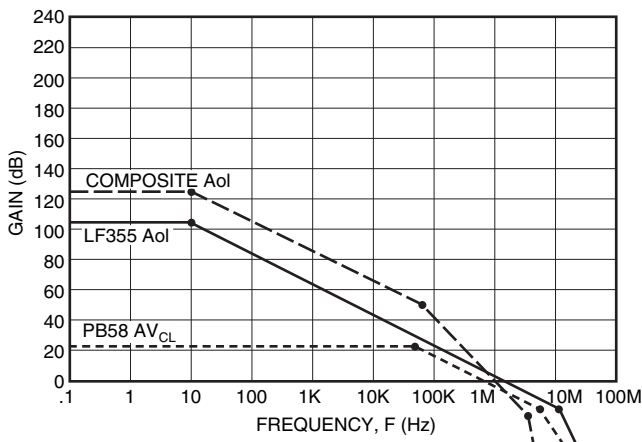


FIGURE 17. CREATION OF COMPOSITE Aol

to drive a 26µF capacitive load. Figure 13 (previous page) illustrates the modified Aol curve with and without the use of Riso. From Figure 14 (back 2 pages) we see -28 degrees of phase margin without R_{ISO}. However, in Figure 15 (previous page) we have 90 degrees of phase margin through the use of R_{ISO}.

STEPS FOR CALCULATING R_{ISO}: (See Figure 13, previous page)

STEP 1: Calculate initial fp: Use Ro and CL which are given by virtue of the load for the application and the choice of power op amp. Plot location of fp.

STEP 2: Graphically choose fz: From plot of fp and fp1 you can see a 40 dB/decade slope heading towards 0 dB gain. Choose fz at a location such that it will change slope of modified Aol from 40 dB/decade to 20 dB/decade for at least a decade above AV_{CL} and within a decade of fp1.

STEP 3: Calculate final value for R_{ISO}: Calculate from formula for fz in Figure 12A the value for R_{ISO} from fz location in Figure 13. Recalculate final value for fp and plot final modified Aol ensuring final location of fz meets criteria in STEP 2.

One disadvantage with the use of R_{ISO} is that the point of feedback is not directly at the capacitive load. This means

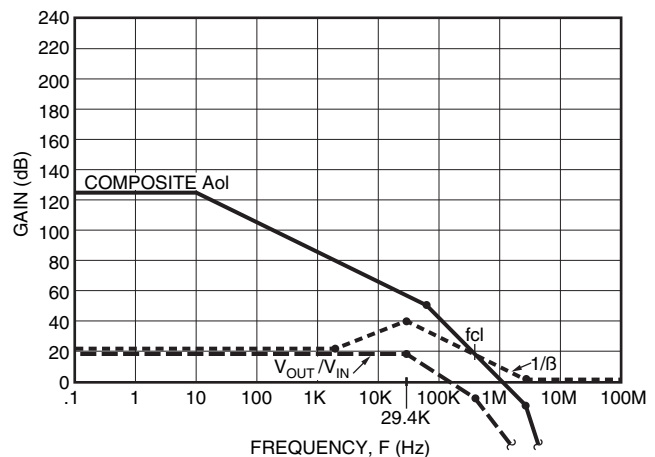


FIGURE 18. COMPOSITE MAGNITUDE PLOT FOR STABILITY

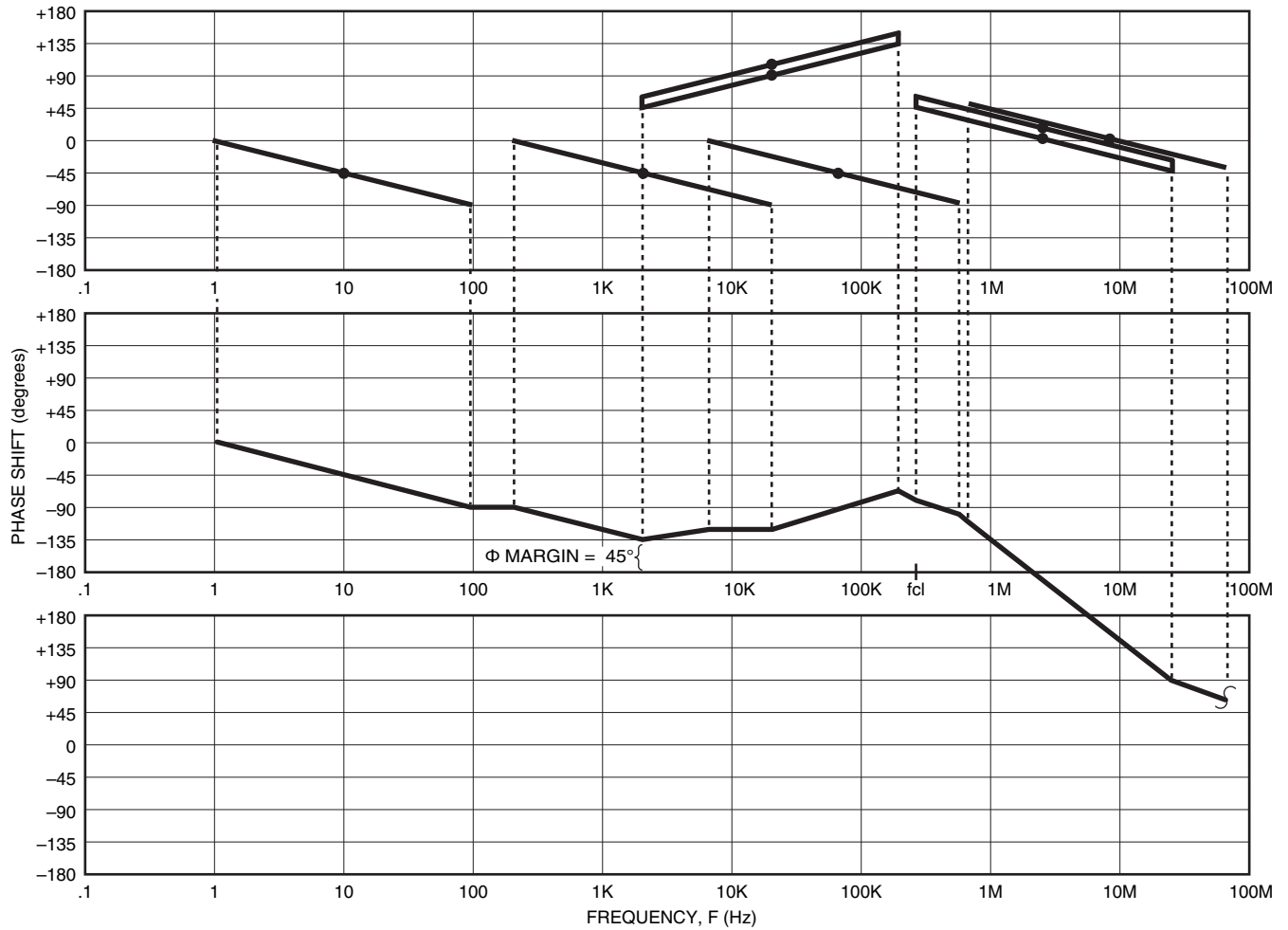


FIGURE 19. COMPOSITE OPEN LOOP PHASE PLOT FOR STABILITY

that accurate control of the voltage at CL is not obtained. This is usually not a problem since most piezo drives are used inside of an outer control loop such as position feedback into a microprocessor which will then generate an error command to the input of the PB58 piezo drive circuit. The major advantage of R_{ISO} is that a wide range of capacitive loads can now be driven with good stability.

3.1.1 PB58 PIEZO DRIVE WITH R_{ISO}

Figure 16 (previous page) is a piezo drive amplifier using the PB58 and our R_{ISO} technique for capacitive load stability.

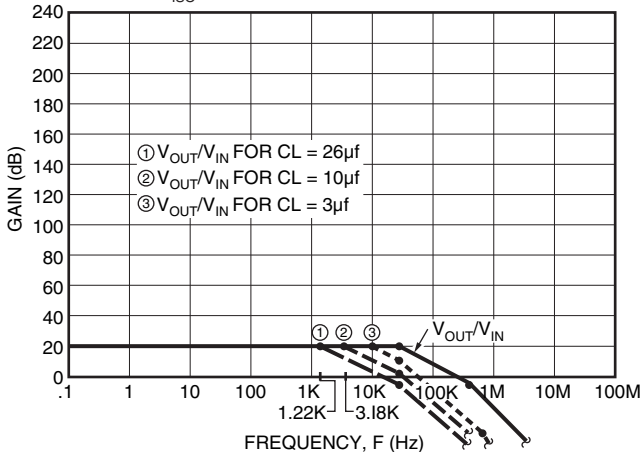


FIGURE 20. V_{OUT}/V_{IN} FOR VARIOUS CL

The design goal for this amplifier was to have an adjustable DC offset and still allow an AC input signal to swing about the DC offset. Amplifier A1 AC couples V_{IN} and offsets it around the selected DC offset set by R_{ADJ} .

The stability of the PB58 composite amplifier begins with first ensuring the PB58 itself is stable. This is accomplished with the use of R_{ISO} in Section 3.1 and Figure 13. Figure 17 (previous page) creates the composite Aol by adding the closed loop

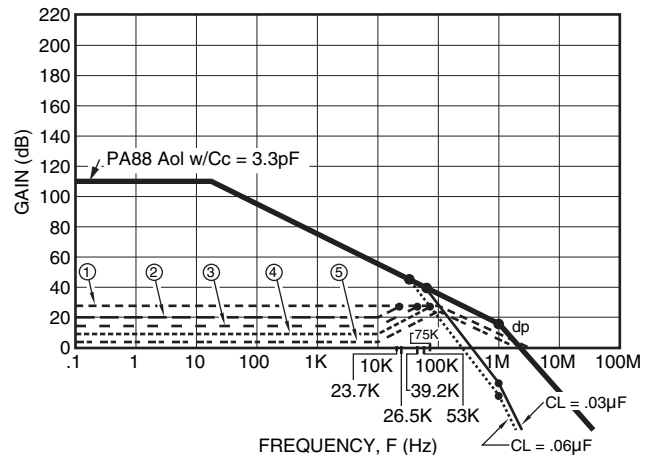
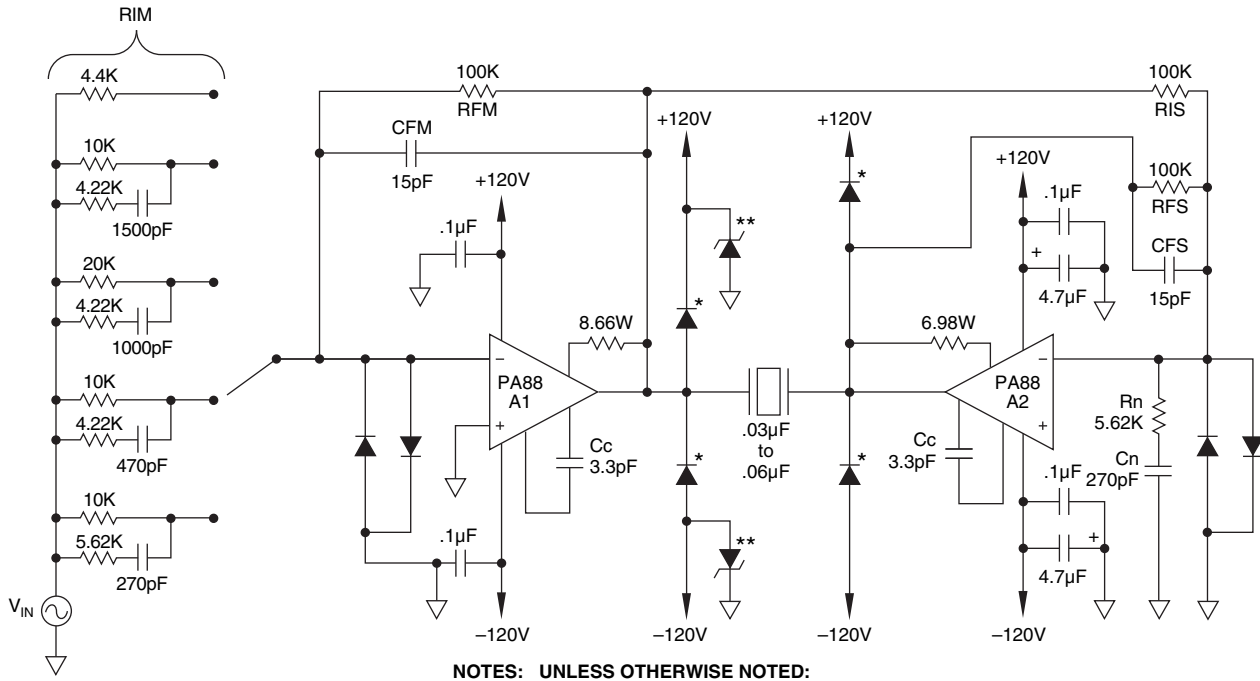


FIGURE 22. A1: MASTER AMPLIFIER MAGNITUDE PLOT FOR STABILITY



- NOTES: UNLESS OTHERWISE NOTED:**
 1) ALL DIODES ARE 1N4148; *DIODES = 1N5617; **TRANSZORBES = 1N6300 or 1.5KE160
 2) USE HS02 HEATSINK @ 25°C AMBIENT

FIGURE 21. PA88 BRIDGE PZT DRIVE WITH SELECTABLE GAIN

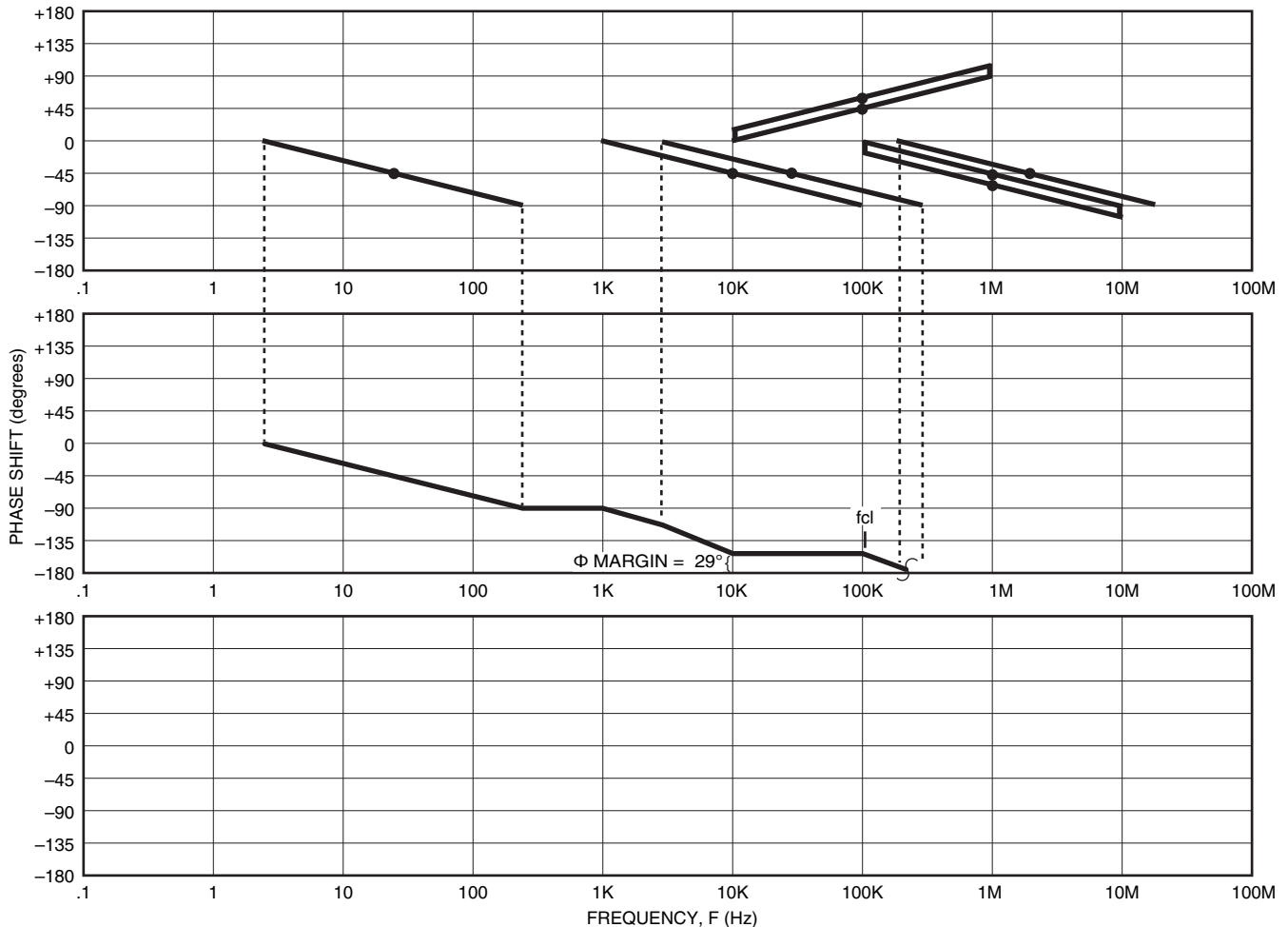


FIGURE 23. A1: MASTER AMPLIFIER OPEN LOOP PHASE PLOT CL = .06mf GAIN = 6dB

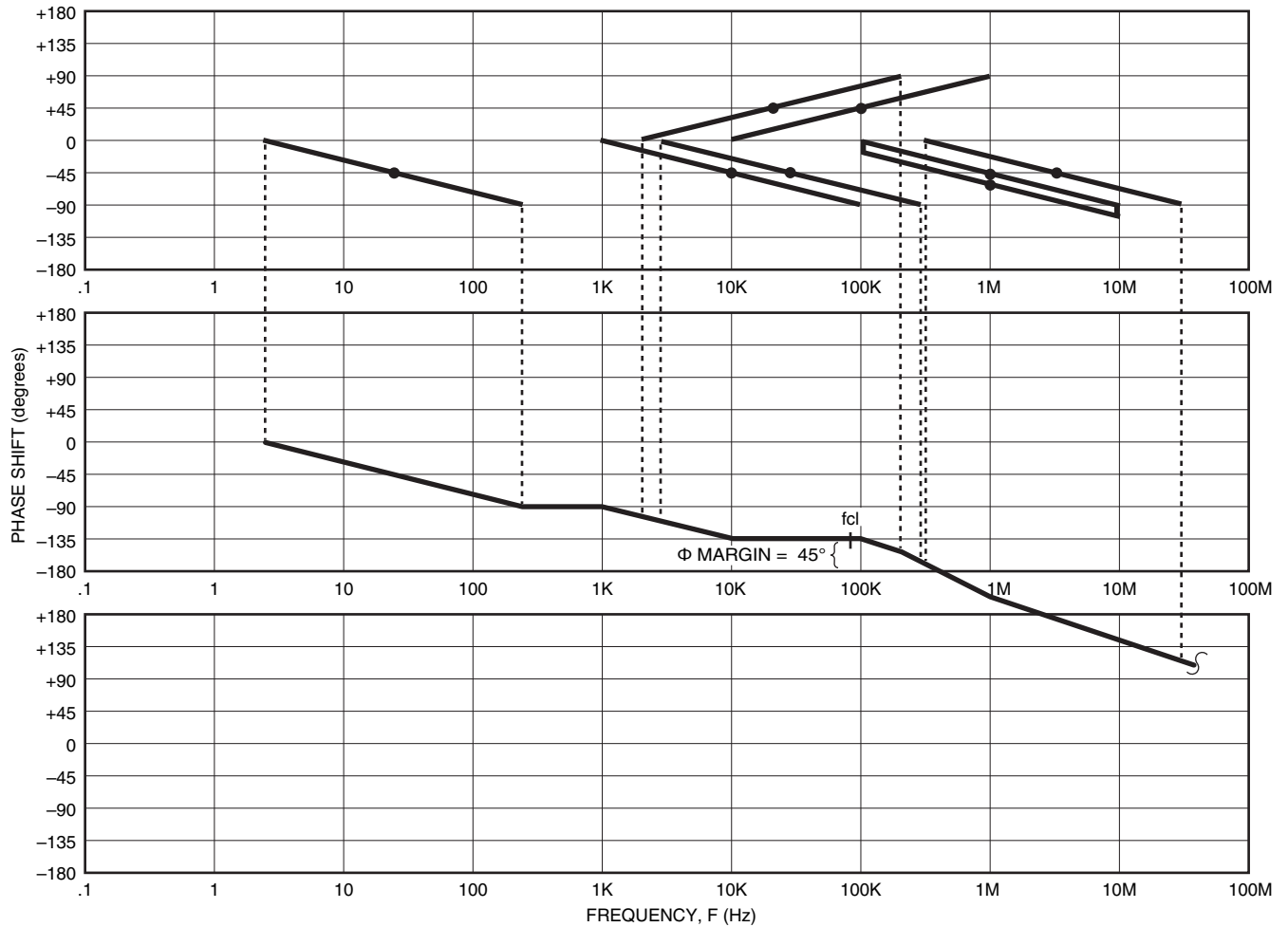


FIGURE 24. A1: MASTER AMPLIFIER OPEN LOOP PHASE PLOT CL = .06 μ F GAIN = 20dB

voltage gain of the PB58 to the open loop gain of the LF355 front end amplifier. For details on stabilizing composite amplifiers, refer to APEX Application Note 19. Figure 18 (back 3 pages) illustrates the 1β plot selected for good stability. Note the V_{OUT}/V_{IN} relationship which will be discussed later. Figure 19 (back 2 pages) verifies good stability through the open loop phase plot.

Since output voltage across CL is not controlled directly, it is of interest to see how the V_{OUT}/V_{IN} relationship changes with capacitive loads. Figure 20 (back 2 pages) shows the V_{OUT}/V_{IN} which is at the output of the amplifier. Curves 1 thru 3 show the effect of the additional V_{OUT}/V_{IN} pole formed by R_{ISO} and CL. As the capacitive load is decreased it's possible to gain a wider bandwidth since the additional pole due to R_{ISO} and CL is moving out higher in frequency.

So far the small signal response for this amplifier has been examined. The large signal response has two limitations. The first is slew rate. The slew rate for the composite is limited to slew rate of the front end times the booster gain. In this case $S.R. = 5V/\mu S \times 10 = 50V/\mu S$. The upper frequency of a sine wave we can track is a 120Vpp sine wave of 133KHz from $S.R. = 2\pi f V_{OP}$. This is not a limiting factor for this circuit since the small signal bandwidth begins to roll off at 28.4 KHz for V_{OUT}/V_{IN} (refer to Figure 20). The second large signal limitation is current drive capability. As the capacitive load is increased, the impedance is lowered as the frequency increases. This translates to higher currents.

The following is lab data taken on the circuit of Figure 16 for power response:

POWER RESPONSE (Ilim = 1.3A)

CL = 10 μ F	f	V_{OUT}
	400Hz	100Vpp
	700Hz	50Vpp
	4KHz	10Vpp

CL = 22 μ F	f	V_{OUT}
	200Hz	100Vpp
	400Hz	50Vpp
	2KHz	10Vpp

Of equal interest is the power supply rejection for this composite since the choice of front end amplifier will change this number to some degree. The following lab data for the circuit of Figure 16 illustrates the PSR for the positive supply.

POSITIVE POWER SUPPLY REJECTION

(DC set for +Vs = +110V, AC set for 2Vpp Ripple)

f	V_{OUT} Ripple	Attenuation	Referred to input	PSR
1KHz	30mVpp	.015	.0015	-56.5db
10KHz	290mVpp	.145	.0145	-36.8db
100KHz	420mVpp	.210	.0210	-33.6db

3.2 CAPACITIVE LOADS AND GAIN SWITCHING

Often times in an end product or test system a customer desires control over the gain setting for the amplifier. With any load this raises some important questions. Capacitive loads only complicate matters somewhat.

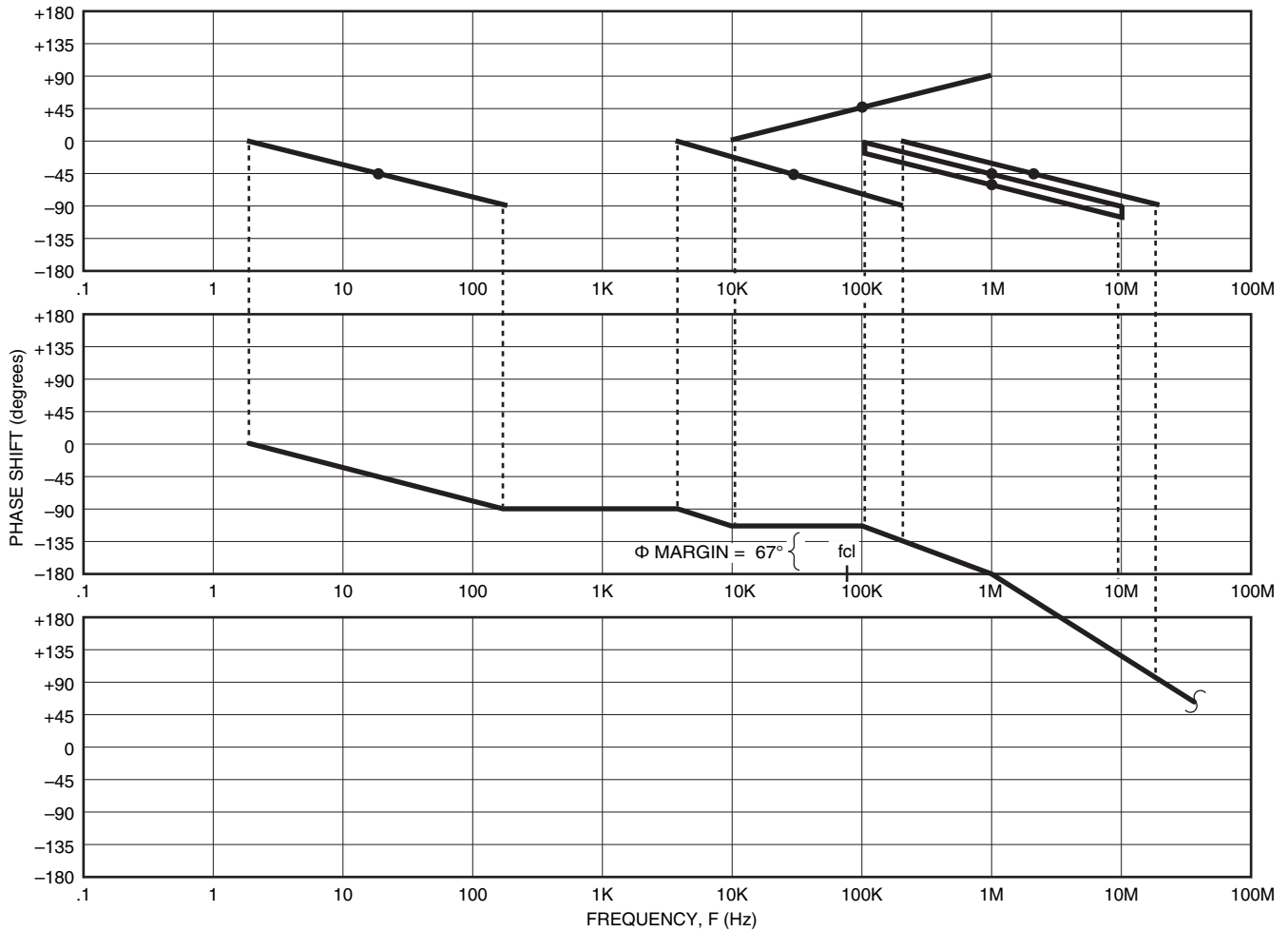


FIGURE 25. A1: MASTER AMPLIFIER OPEN LOOP PHASE PLOT
 $CL = .06\mu F$ GAIN = 27.5 dB

Figure 21 (previous page) shows a bridge circuit for driving piezo transducers. The bridge circuit allows up to twice the peak voltage across the load than driving the load ground

referenced. This is because as A1 goes towards +120V, A2 drives towards -120V yielding up to twice the peak voltage across the load. Correspondingly, the bridge circuit also

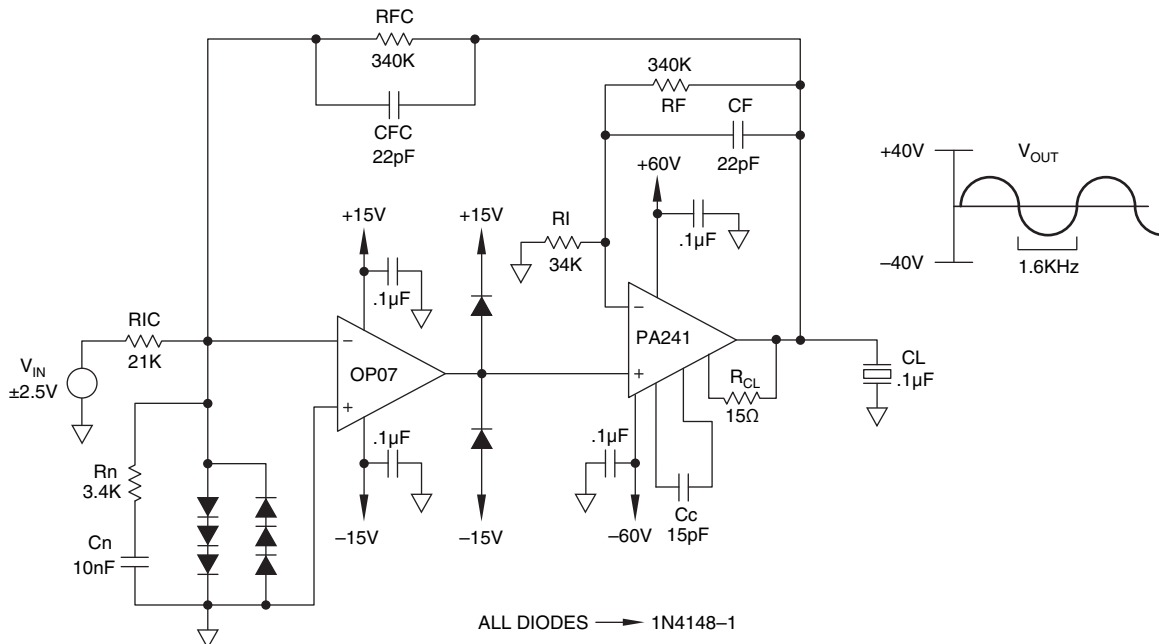


FIGURE 26. PA241 COMPOSITE PIEZO TRANSDUCER DRIVE

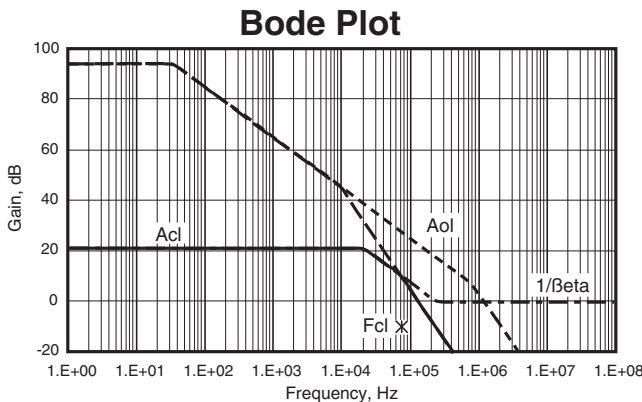
doubles the voltage slew rate across the load for the same reason. Forcing the master amplifier, A1, to current limit first, equally distributes SOA stresses between A1 and A2 in case of a shorted load.

A range of loads was defined for this amplifier as shown in Figure 21 (back 3 pages). The key to successfully changing the gains in this circuit is to change the noise gain compensation components as the input resistor is changed to select the desired gain setting. It is HIGHLY RECOMMENDED NOT to switch in different values of Cc around the PA88 amplifier A1 as gains are changed. There are MOSFET gates that are connected to the compensation pins that could be destroyed with compensation capacitor switching. It is also critical for stability that Cc be located directly at the amplifier which does not yield itself easily to switching. Figure 22 (back 4 pages) illustrates the 1/β plots for stability for all selectable gain settings. Notice that the stability technique applied here uses both noise gain compensation on the input along with the feedback zero to maximize phase margin for stability. The modified Aol curves are shown for CL = .06μF and CL = .03μF. Output impedance for the PA88 of 100 ohms was used. Figures 23, (back 3 pages) 24, (back 2 pages) and 25 (previous page) prove through open loop phase plots that good stability is guaranteed. Open loop phase plot for A2 will be the same as Figure 23.

3.3 HIGH ACCURACY, HIGH VOLTAGE, LOW COST PZT DRIVE

Figure 26 (previous page) is an example of a high accuracy (input offset = 60μV), low drift high voltage amplifier. Though only used here at +/-60V, the PA241 can be used up to +/-175V supplies. The PA241 is a low cost monolithic ASIC designed for high voltage. The limitations of the high voltage ASIC technology do not allow for optimization of input characteristics, thus the PA241 has a 40mV input offset voltage. In high voltage applications where low drift or high accuracy are desired this can be accomplished through the use of a composite amplifier which uses a low cost monolithic front end amplifier to

MODEL	PA241,3-150	Note/PBs	Rn	9999999999	Kohms
Rcl	15	Ohms	Cn	0	nF
Cload	0.1	uF	Cf	22	pF
Rin	34	Kohms	Riso	0	Ohms
Rf	340	Kohms			



Total Rout	165	Ohms
Pole Zout/Cload	9.645744481	KHz
1/Beta (DC)	20.8	dB
Noise Gain	0.0	dB
Pole Noise Gain	0.159154943	KHz
Zero Noise Gain	0.159154938	KHz
Pole Cf/Rf	21.27739784	KHz
Zero Rf/Cf	234.051377	KHz
Zero Riso/Cload	1.59155E+11	KHz

FIGURE 27.

control accuracy and drift. The PA241 now acts as a voltage and current booster.

There are three simple steps to stabilize a composite with a capacitive load:

STEP 1: Compensate PA241 for stability first: Refer to Figure 27 which shows how capacitive load modifies Aol. Figure 28 confirms that the selected 1/β plot will guarantee stability for the PA241.

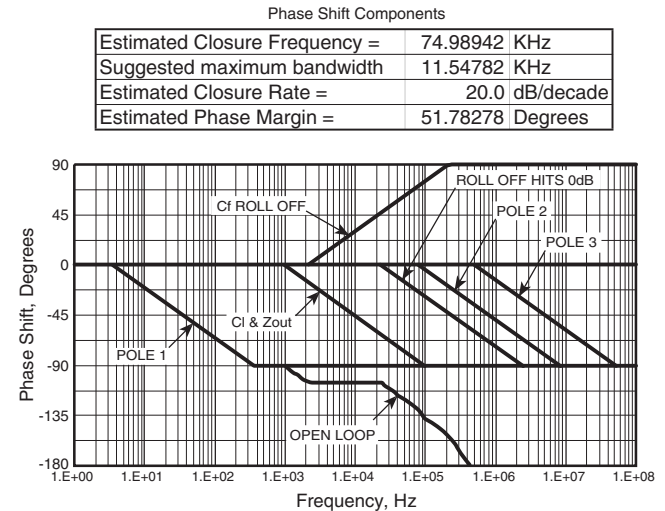


FIGURE 28.

STEP 2: Create composite Aol: Refer to Figure 29 which shows addition of closed loop gain of PA241 to OP07 Aol on dB plot to yield net Composite Aol.

MODEL	OP07	READ ME		
Aol =	135	dB	Pole 1 =	0.1 Hz
Pole 2 =	7.00E+05	Hz	Pole 3 =	7.00E+06 Hz
Rin	21	Kohms	Rn	999999999 Kohms
Rf	340	Kohms	Cn	0 nF
Cf	0	pF	Using Look-Up data	

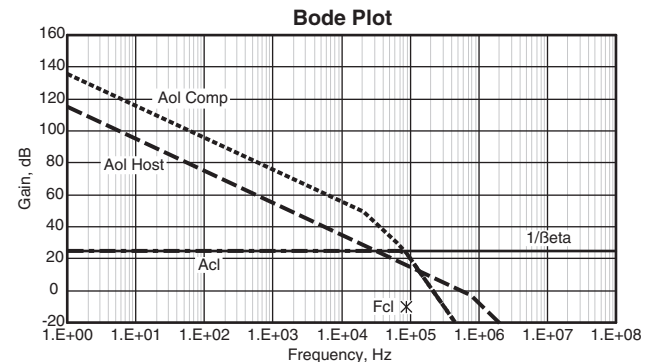


FIGURE 29.

STEP 3: Compensate composite op amp: Figure 30 (see next page) shows the selected 1/β plot to stabilize composite amplifier. Both noise gain compensation and feedback zero compensation are used to maximize stability. Figure 31 (see next page) plots the open loop phase for the composite amplifier yielding 50 degrees phase margin and good stability.

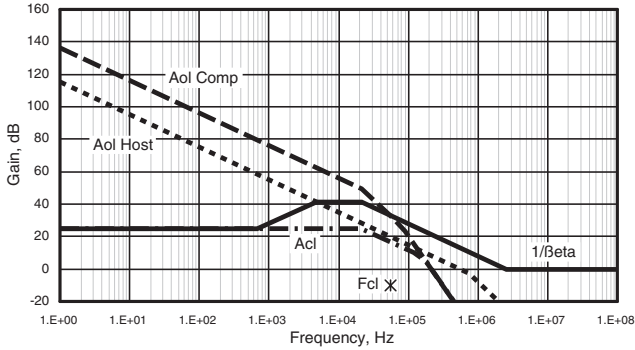
3.4 HIGH HIGH VOLTAGE AMPLIFIER CIRCUIT

Figure 32 (see next page) illustrates the current state of the industry with regards to highest voltage available using op amps. This bridge circuit will give us up to +/-1160V across the load.

Remember when using the PA89 to pay particular attention to input protection, heatsinking (low quiescent current times high

MODEL	OP07	READ ME		
Aol =	135	dB	Pole 1 =	0.1 Hz
Pole 2 =	7.00E+05	Hz	Pole 3 =	7.00E+06
Rin	21	Kohms	Rn	3.4 Kohms
Rf	340	Kohms	Cn	10 nF
Cf	22	pF	Using Look-Up data	

Bode Plot



1/Beta (DC)	24.7	dB
Noise Gain	16.7	dB
Pole Noise Gain	4.681027677	KHz
Zero Noise Gain	0.68665214	KHz
Pole Cf/Rf	21.27739871	KHz
Zero Rf/Cf	2493.508487	KHz

FIGURE 30.

Estimated Closure Frequency =	56.23413	KHz
Suggested maximum bandwidth	5.623413	KHz
Estimated Closure Rate =	20.0	dB/decade
Estimated Phase Margin =	50.625	Degrees

Phase Shift Components

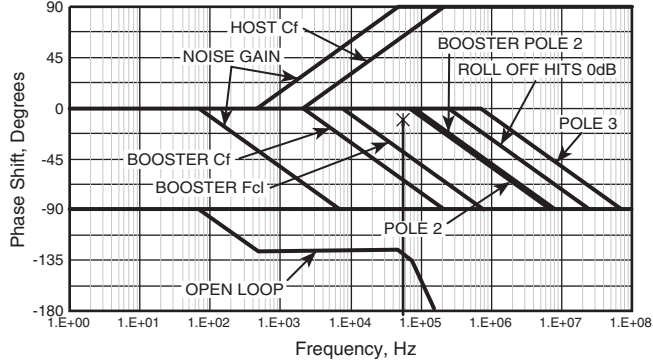


FIGURE 31.

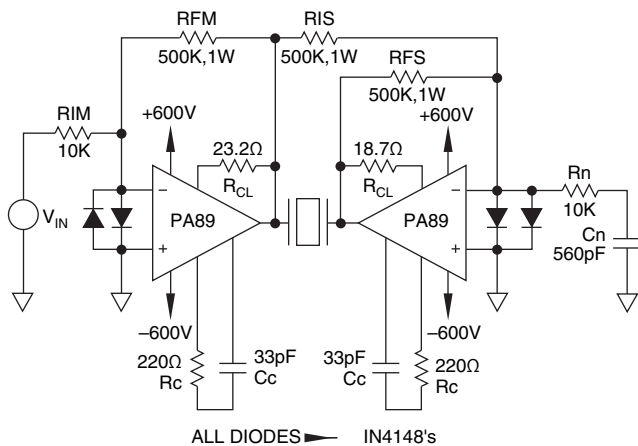


FIGURE 32. ±1160V PIEZO DRIVE BRIDGE

voltage ==> power dissipation!), components (power dissipation and voltage coefficient of resistance), and compensation capacitor (1200V rating necessary).

3.5 860VPP SINGLE SUPPLY PIEZO DRIVE

Occasionally it is desired to provide a bipolar drive to a capacitive load using only a single supply. This will reduce area and cost by only requiring one power supply. It will however require the use of a bridge circuit with two high voltage amplifiers.

Figure 33 (next page) is an implementation of an 860Vpp piezo drive. There are four simple steps to setting up the single supply scaling:

STEP 1: Define maximum V_{OP} :

$$MAX V_{OP} = +V_s - V_{satA} - V_{satB}$$

$$MAX V_{OP} = +450 - 10V - 10V = 430Vp$$

STEP 2: Calculate gain:

$$Gain = V_{OPP} / V_{INPP} = (V_A - V_B)_{pp} / V_{INPP}$$

$$Gain = 860V_{pp} / 12V_{pp} = 71.67$$

Gain = 2 RF/RI with the bridge configuration. That is the voltage gain across the load is twice that of the master amplifier, A, since +1V out of amplifier A yields -1V out of amplifier B, relative to the midpoint power supply reference of +225V. Therefore: RF/RI = 71.67/2 = 35.833

STEP 3: Calculate offset:

$$V_A - V_B = +V_s(2(1 + RF/RI)\left(\frac{R_B}{R_A + R_B}\right) - 1) - 2(RF/RI)V_{IN}$$

But when $V_{IN} = 0$ then $V_A - V_B = +430V$

Using RF/RI = 35.833 and solving above equation yields $RA = 36.669RB$

Choosing $RB = 12K$ implies $RA = 440K$

STEP 4: Check for common mode voltage compliance:

The resistor divider of RA and RB was set to yield the desired offset. These values yield $V_r = 11.95V$ which is greater than the minimum common mode voltage specification of 10V for the PA85.

4.0 FINAL NOTE

You have now looked at several ways to drive capacitive loads using high voltage amplifiers. The techniques presented here are intended to enable you to complete your circuit designs in a short time.

If there are additional questions or concerns not covered in this application note, please feel free to contact APEX APPLICATIONS ENGINEERING through our TOLL FREE HOTLINE, 800-546-2739 (Canada & USA, outside Arizona), by direct telephone, 520-690-8600, or by using the APEX APPLICATIONS FAX, 520-888-7003.

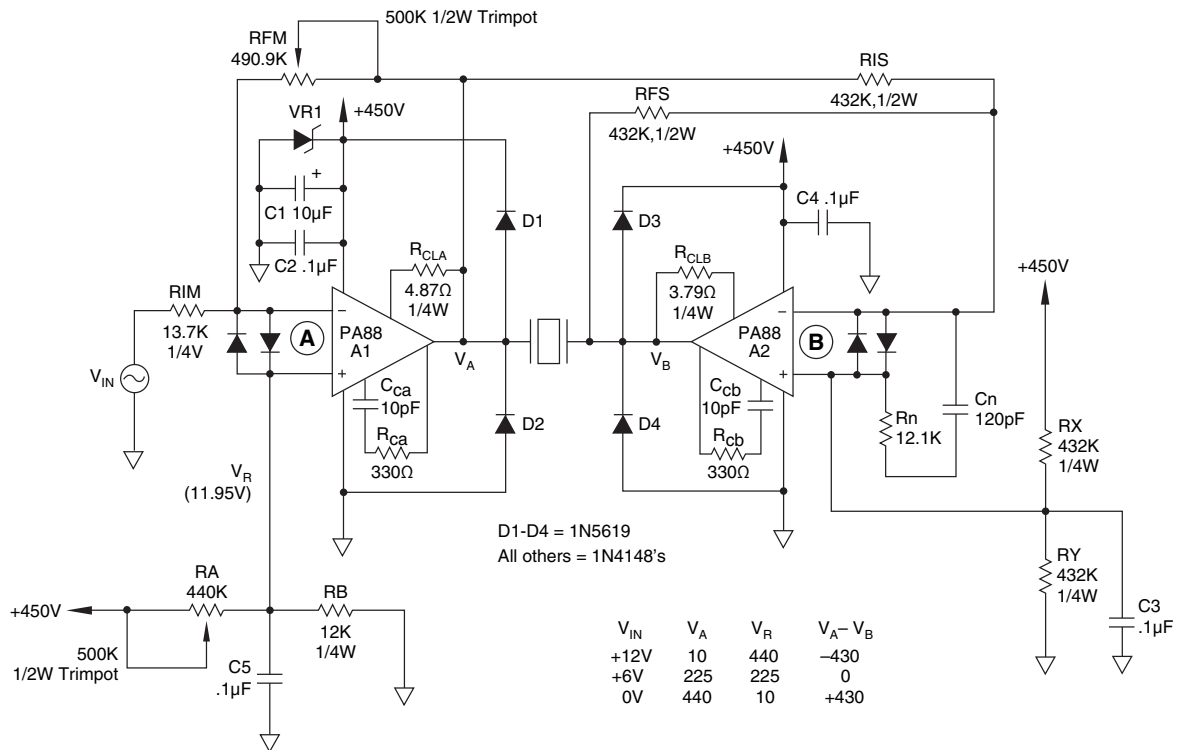


FIGURE 33. 860Vpp PIEZO DRIVE
(SINGLE SUPPLY BRIDGE)

